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EXAMINER	
CHEN, ERIC BRICE	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,318	MUI ET AL.	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *1-7 and 28-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-30* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-2 and 28-30 drawn to an etching system, classified in class 156, subclass 345.1.

   II. Claims 3-7, drawn to a method for etching a feature, classified in class 438, subclass 706.

   III. Claims 8-27, drawn to a method for etching a mask, classified in class 438, subclass 735.

2. The inventions are distinct, each from the other because of the following reasons: Inventions I-III are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different modes of operation, different functions, or different effects (MPEP § 806.04, MPEP § 808.01).

3. Invention I is drawn to an etching system, which is not the subject of the other inventions in Inventions II-III. Etching of a feature on a substrate or trimming the patterned mask does not require the claimed etching system.

4. Invention II is drawn to a method for etching a feature, which is not the subject of the other inventions in Inventions I, III. Etching of a feature on a substrate does not require trimming the patterned mask and does not require the claimed etching system.

5. Invention III is drawn to a method for etching a feature, which is not the subject of the other inventions in Inventions I-II. Etching of a feature on a substrate or trimming the patterned mask does not require the claimed etching system.

6. Because these inventions are distinct for the reasons given above and the search required for Invention I is not required for Inventions II-III, the search required for Invention II is not required for Inventions I, III, and the search required for Invention III is not required for Inventions I-II. Moreover, because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

7. During a telephone conversation with Keith Taboada on June 20, 2005, a provisional election was made without traverse to prosecute Invention III, claims 8-27. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1-7 and 28-30 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

8. Applicants are reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Priority

9. Applicant is advised of possible benefits under 35 U.S.C. 119(a)-(d), wherein an application for patent filed in the United States may be entitled to the benefit of the filing date of a prior application filed in a foreign country.

Double Patenting

10. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

11. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

12. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

13. Claims 8-11 and 16-19 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 7-8, 10, 12, and 19-20 of copending Application No. 10/666,317, Mui et al. (U.S. Patent Appl. Pub. No. 2005/0064714) in view of Tao et al. (U.S. Patent No. 6,620,631) ("Tao I"). This is a provisional obviousness-type double patenting rejection.

14. As to claim 8, Mui claims a method for controlling accuracy and repeatability of an etch process, comprising: (a) providing a batch of substrates, each substrate having a patterned mask formed on a film stack comprising at least one material layer (Application No. 10/666,317, filed Sept. 19, 2003, claim 1, page 16, line 5); (b) measuring dimensions of elements of the patterned mask on at least one substrate of the batch of substrates (claim 1, page 16, line 6); and (d) etching the at least one material layer on the at least one substrate (claim 1, page 16, lines 9-10); and (f) adjusting the process recipe of step (d) based on the measurements performed (claim 1, page 16, lines 7-8).

15. The claims of Mui fail to include the limitations of: (c) trimming the patterned mask on the at least one substrate using a process recipe based on the measurements performed at step (b); (e) measuring dimensions of etched structures formed on the at least one substrate during step; and (f) adjusting the process recipe of step (c) based on the measurements performed at step (e), as required by Applicants' claim 8. Tao I teaches a method of enhancing linewidth control and critical dimension during semiconductor fabrications (column 1, lines 22-26), including establishing a correlation relating the pattern masked layers with optical measurements, determining a deviation,

and compensating for the deviation (column 8, lines 62-67), including adjusting the trimming of the patterned masking (column 9, lines 20-28). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the steps of (c) trimming the patterned mask on the at least one substrate using a process recipe based on the measurements performed at step (b); (e) measuring dimensions of etched structures formed on the at least one substrate during step; and (f) adjusting the process recipe of step (c) based on the measurements performed at step (e). One who is skilled in the art would be motivated to adopt a process for enhancing linewidth control and critical dimension during semiconductor fabrications.

16. As to claim 9, Mui claims that the steps (b) and (e) use an optical measuring technique (claim 7, page 16, lines 26-27).

17. As to claim 10, the claims of Mui fail to include the limitation that the optical measuring technique is a scatterometric measuring technique. However, Tao I discloses that any optical method may be used for measuring patterned masked layers (column 8, lines 59-61). Moreover, Tao I teaches that a scatterometer apparatus has been used successfully in characterizing the surface microelectronic device during fabrication (column 3, lines 1-11). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a scatterometric measuring technique. One who is skilled in the art would be motivated to use an optical technique, such scatterometric measuring, which has been previously demonstrated to accomplish the task of characterizing the surface of a microelectronic device.

18. As to claim 11, Mui claims that the steps (b) through (e) are performed using processing modules of a single substrate processing system (claim 8, page 16, lines 29-30).

19. As to claim 16, Mui claims a method for controlling accuracy and repeatability during formation of a gate structure of a field effect transistor (claim 12, page 17, lines 13-14), comprising: (a) providing a batch of substrates, each substrate having a patterned mask formed on a gate electrode layer of the gate structure (claim 12, page 17, lines 15-16); (b) measuring dimensions of elements of the patterned mask on at least one substrate of the batch of substrates (claim 12, page 17, line 18); (d) etching the gate electrode layer on the at least one substrate (claim 12, page 17, lines 21-22); and (f) adjusting the process recipe of step (d) based on the measurements performed (claim 12, page 17, lines 19-20).

20. The claims of Mui fail to include the limitations of: (c) trimming the patterned mask on the at least one substrate using a process recipe based on the measurements performed at step (b); (e) measuring dimensions of etched gate electrode structures formed on the at least one substrate during step (d); and adjusting the process recipe of step (c) based on the measurements performed at step (e), as required by Applicants' claim 16. Tao I teaches a method of enhancing linewidth control and critical dimension during semiconductor fabrications (column 1, lines 22-26), including establishing a correlation relating the pattern masked layers with optical measurements, determining a deviation, and compensating for the deviation (column 8, lines 62-67), including adjusting the trimming of the patterned masking (column 9, lines 20-28). Therefore, it

would have been obvious to one of ordinary skill in the art at the time the invention was made to include the steps of (c) trimming the patterned mask on the at least one substrate using a process recipe based on the measurements performed at step (b); (e) measuring dimensions of etched gate electrode structures formed on the at least one substrate during step (d); and adjusting the process recipe of step (c) based on the measurements performed at step (e). One who is skilled in the art would be motivated to adopt a process for enhancing linewidth control and critical dimension during semiconductor fabrications.

21. As to claim 17, Mui claims that the steps (b) and (e) use an optical measuring technique (claim 19, page 18, lines 7-8).

22. As to claim 18, the claims of Mui fail to include the limitation that the optical measuring technique is a scatterometric measuring technique. However, Tao I discloses that any optical method may be used for measuring patterned masked layers (column 8, lines 59-61). Moreover, Tao I teaches that a scatterometer apparatus has been used successfully in characterizing the surface microelectronic device during fabrication (column 3, lines 1-11). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a scatterometric measuring technique. One who is skilled in the art would be motivated to use an optical technique, such scatterometric measuring, which has been previously demonstrated to accomplish the task of characterizing the surface of a microelectronic device.

23. As to claim 19, Mui claims that the steps (b) through (e) are performed using processing modules of a single substrate processing system (claim 20, page 18, lines 10-11).

Claim Rejections - 35 USC § 102

24. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

25. Claims 8-9, 11-14, 16-17, 19-22, and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Tao I.

26. As to claim 8, Tao I discloses a method for controlling accuracy and repeatability of an etch process, comprising: (a) providing a batch of substrates, each substrate (10) (column 6, lines 37-41) having a patterned mask (14a/14b/14c/14d/14e) (column 7, lines 35-37) formed on a film stack comprising at least one material layer (12) (column 6, lines 34-36); (b) measuring dimensions of elements of the patterned mask (14a/14b/14c/14d/14e) on at least one substrate (10) (column 8, lines 50-61) of the batch of substrates (column 8, lines 62-67); (c) trimming the patterned mask (14a/14b/14c/14d/14e) (column 9, lines 20-28) on the at least one substrate using a process recipe based on the measurements performed at step (b) (column 8, lines 62-

67; column 9, lines 1-15); (d) etching the at least one material layer on the at least one substrate (column 9, lines 1-4); (e) measuring dimensions of etched structures formed on the at least one substrate during step (d) (column 9, lines 4-12); and (f) adjusting the process recipe of step (c) (column 9, lines 11-15, lines 26-28) or/and the process recipe of step (d) based on the measurements performed at step (e) (column 9, lines 4-15).

27. As to claim 9, Tao I discloses that the steps (b) and (e) use an optical measuring technique (column 8, lines 50-61).

28. As to claim 11, Tao I discloses that steps (b) through (e) are performed using processing modules of a single substrate processing system (column 5, lines 38-44).

29. As to claim 12, Tao I discloses that the step (f) further comprises: modifying a time duration or process parameters for trimming the patterned mask (column 9, lines 20-28).

30. As to claim 13, Tao I discloses that the step (f) further comprises: modifying a time duration or process parameters for etching the material layer (column 9, lines 4-15).

31. As to claim 14, Tao I discloses the step (d) further comprises: compacting/outgassing or removing at least a portion of post-etch residue formed on sidewalls of the etched structures (column 9, lines 20-32).

32. As to claim 16, Tao I discloses a method for controlling accuracy and repeatability during formation of a gate structure of a field effect transistor (column 5, lines 56-63), comprising: (a) providing a batch of substrates, each substrate (10) having a patterned mask (14a/14b/14c/14d/14e) (column 7, lines 35-37) formed on a gate

electrode layer of the gate structure; (b) measuring dimensions of elements of the patterned mask (12) (column 7, lines 21-31; Figure 1) on at least one substrate of the batch of substrates (column 8, lines 62-67); (c) trimming the patterned mask (14a/14b/14c/14d/14e) (column 9, lines 20-28) on the at least one substrate using a process recipe based on the measurements performed at step (b) (column 8, lines 62-67; column 9, lines 1-15); (d) etching the gate electrode layer on the at least one substrate (column 9, lines 1-4); (e) measuring dimensions of etched gate electrode structures formed on the at least one substrate during step (d) (column 9, lines 4-12); and (f) adjusting the process recipe of step (c) (column 9, lines 11-15, lines 26-28) or/and the process recipe of step (d) based on the measurements performed at step (e) (column 9, lines 4-15).

33. As to claim 17, Tao I discloses that the steps (b) and (e) use an optical measuring technique (column 8, lines 50-61).

34. As to claim 19, Tao I discloses that the steps (b) through (e) are performed using processing modules of a single substrate processing system (column 5, lines 38-44).

35. As to claim 20, Tao I discloses that the step (f) further comprises: modifying a time duration or process parameters for trimming the patterned mask (column 9, lines 20-28).

36. As to claim 21, Tao I discloses that the step (f) further comprises: modifying a time duration or process parameters for etching the material layer (column 9, lines 4-15).

37. As to claim 22, Tao I discloses that the gate electrode layer (12) comprises doped polysilicon (column 7, lines 21-25).

38. As to claim 24, Tao I discloses the step (d) further comprises: compacting/outgassing or removing at least a portion of post-etch residue formed on sidewalls of the etched structures (column 9, lines 20-32).

Claim Rejections - 35 USC § 103

39. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

40. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

41. Claims 10 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tao I.

42. As to claims 10 and 18, Tao I does not expressly disclose that the optical measuring technique is a scatterometric measuring technique. However, Tao I discloses that any optical method may be used (column 8, lines 59-61). Moreover, Tao I teaches that a scatterometer apparatus has been used successfully in characterizing the surface microelectronic device during fabrication (column 3, lines 1-11). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a scatterometric measuring technique. One who is skilled in the art would be motivated to use an optical technique, such scatterometric measuring, which has been previously demonstrated to accomplish the task of characterizing the surface of a microelectronic device.

43. Claims 15, 23, and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tao I in view of Tao et al. (U.S. Patent No. 6,242,350) ("Tao II").

44. As to claims 15 and 25, Tao I does not expressly disclose thinning the post-etch residue to a thickness of less than about 10 nm. Tao II teaches that etching polysilicon with HBr results in the deposition of polymer residue (56/58/60) (column 5, lines 8-14; Figure 4). Moreover, Tao II teaches that the polymer reside can be removed by dry etching with nitrogen (N_2), oxygen (O_2) and hydrogen (H_2) (column 6, lines 64-67). However, this etching step also etches the gate oxide (column 5, lines 18-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to thin the post-etch residue to a thickness of less than about 10 nm. One who is skilled in the art would be motivated to remove the residue, but not overetch the gate oxide.

45. As to claim 23, Tao I does not expressly disclose that the step (d) further comprises: providing HBr and Cl_2 at a flow ratio HBr:Cl_2 in a range from 1:15 to 15:1. However, Tao II discloses a method of etching polysilicon layer (46) overlying gate oxide (42) (Figure 3) with HBr and Cl_2 at a flow ratio HBr:Cl_2 in a range from 1:15 to 15:1 (column 4, lines 31-54). Moreover, Tao II teaches that the flow ratio HBr:Cl_2 is varied in order to achieve a desired polysilicon/oxide selectivity, to avoid overetching the gate oxide (42) (column 4, lines 44-49). Therefore, it would have obvious to one of ordinary skill in the art to provide HBr and Cl_2 at a flow ratio HBr:Cl_2 in a range from 1:15 to 15:1. One who is skilled in the art would adopt an etching method that avoids overetching of an underlying gate oxide.

46. As to claim 26, Tao I does not expressly disclose using a plasma comprising one or more gases selected from the group consisting of nitrogen (N_2), oxygen (O_2) and hydrogen (H_2). Tao II teaches that etching polysilicon with HBr results in the deposition of polymer residue (56/58/60) (column 5, lines 8-14; Figure 4). Moreover, Tao II teaches that the polymer reside can be removed by dry etching with nitrogen (N_2), oxygen (O_2) and hydrogen (H_2) (column 6, lines 64-67). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to using a plasma comprising one or more gases selected from the group consisting of nitrogen (N_2), oxygen (O_2) and hydrogen (H_2). One who is skilled in the art would be motivated to remove polymer residue after the etching polysilicon with HBr.

47. As to claim 27, Tao II discloses providing nitrogen (N_2) and hydrogen (H_2) at a N_2:H_2 flow ratio in a range from 3:1 to 100% of N_2 (column 7, lines 1-4); maintaining the

substrate at a temperature between about 200 and 350 degrees Celsius (column 7, lines 27-28; Table II); applying power to an inductively coupled power source between about 1000 and 7000 W (column 7, lines 23-24; Table II); and maintaining a chamber pressure between about 500 and 2000 mTorr (column 7, lines 22-23; Table II).

Conclusion

48. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Stirton (U.S. Patent No. 6,479,200) discloses a method of controlling photoresist exposure by scatterometric techniques. Bonser et al. (U.S. Patent No. 6,245,581) discloses a method for controlling the critical dimensions of a semiconductor device. Lensing et al. (U.S. Patent No. 6,433,871) discloses scatterometry measurements to control gate electrode profiles. Lensing (U.S. Patent No. 6,707,562) discloses using scatterometry measurements to control photoresist etch process.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC

EBC
June 21, 2005

NADINE G. NORTON
SUPERVISORY P